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EXAMINER	
SAXENA, AKASH	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/023,235	BERNSTEIN ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-22 and 24-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-11, 13-22, 24-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-3, 5-11, 13-22, 24-42 has/have been presented for examination based on amendment filed on 27th March 2007.
2. Claim(s) 1-3, 5-11, 13-19, 24-25, 35-37, and 40 is/are amended.
3. Claim(s) 4, 12, 23 is/are cancelled.
4. Claim(s) 41-42 is/are new claim(s) added with this amendment.
5. Claim(s) 1-3, 5-11, 13-22, 24-42 remain rejected under 35 USC § 112.
6. Claim(s) 1-3, 5-11, 13-22, 24-42 remain rejected under 35 USC § 103.
7. The arguments submitted by the applicant have been fully considered. Claims 1-3, 5-11, 13-22, 24-42 remain rejected and this action is made FINAL. The examiner's response is as follows.

Claim Interpretation

Regarding Claim 1

8. The phrase "performance parameter" is understood as the current voltage switch-point of a transistor computer model in reference to claim and as understood from specification [0018].
9. The phrase "second bounded range" is a range representing the variation in the "performance parameter" due to variation in the design of device. In other words, second bounded range represents a range of current voltage switch points of a transistor computer model due to variations in designs of a transistor. For example variations in design of transistor is understood as change in length & width of transistor.

Regarding Claim 19

10. The "primary parameters" of a feature as disclosed in the specification ([0039]) are performance characteristics that are directly related to the specific physical feature. For example, in MOSFET designs, the overlap capacitance (C.sub.ov) is directly related to the length of the physical overlap of the gate material over the diffusion and extension (or lightly-doped drain) implants and the gate oxide thickness.

11. The "secondary parameters" of a feature, as disclosed in the specification ([0040]-[0041]) are calculated based on the one or more primary parameters. Fir example total gate capacitance.

Response to Applicant's Remarks for 35 U.S.C. § 103

12. Claim(s) 1, 9, 14, 19, 24, 36, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hershenson, in view of Krivokapic.

Regarding Claim 1, 9, 14, 19, 24, 36, 40 and 42

(Argument 1) Applicant has argued, "Nowhere in Hershenson does it disclose a target performance parameter range".

(Response 1) Examiner respectfully disagrees. Please see Hershenson below.

Hershenson Col.3 Line 67-Col.4 Line 39 - where the performance specifications for the integrated circuit topologies are described as posynomial functions of the design parameters (i.e. target performances). The performance specifications are combined with user defined design objectives and constraints to form a geometric program. One embodiment reformulates geometric programs as convex optimization problems, i.e., the problem of minimizing a convex function subject to convex inequalities constraints and linear equality constraints;

Hershenson Col.7 Lines 30-50 - where the optimization problem based on the performance posynomial is expressed as an inequality bounded by range "less than or equal to one".

Hershenson Col.21 Lines 44-58 - where the (target parameter) performance can be handled in ranges.

(Argument 2) Applicant has argued, "Nowhere in Krivokapic is a target performance parameter range disclosed."

(Response 2) Teachings of Hershenson are used to teach target performance parameter in broadest possible interpretation – see argument 1 above.

(Argument 3) Applicant has argued, "Neither Krivokapic, nor Hershenson teach the limiting feature that the target performance range includes *first bounded ranges* each comprising range of performance parameter variations due to manufacturing process variations and each based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point."

(Response 3) Examiner respectfully disagrees, as combined teachings of Hershenson and Krivokapic teach the above limitations. First, Hershenson teaches *bounded range* for the process variations (See response to argument 1). As for process variations based on a corresponding one of the multiple model curves for different designs of said device, Hershenson teaches various circuit topologies performing the same function but optimized for various performance points (Hershenson: at least Col.5 Lines 40 –Col.6 Lines 24). Applicant's interpretation of topology is noted, however, the broadest reasonable interpretation of the claim language "different designs" includes the examiner's interpretations. Applicant's argument that "different design" should be interpreted as disclosed in [0025], referring to different technology is not present in claim. Examiner maintains the broadest interpretations and presents Hershenson where 3 possible device models are presented based on the circuit design (Hershenson: Col.6 Lines 1-24). Further to

address the newly added limitation that "multiple first bounded ranges" representing the process variation for the target performance parameter, are taught by at least by Krivokapic (Krivokapic: See Fig.1) where the separate parameters 103-107 are presented to the device simulator leading to bound ranges 110 and multiple curves 109.

(Argument 4) Applicant has argued, "Nor do they (Hershenson and Krivokapic) teach or suggest that the target performance parameter also include a second bound range that is constrained by *at least two multiple model curves*".

(Response 4) As shown Hershenson teaches performance analysis for at least 3 models (Hershenson: Col.6 Lines 1-24), thereby meeting the limitation of the second bound ranges. Krivokapic also teaches the above limitation (Krivokapic: Col.8 Lines 50-63).

Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive.

Claim Objections

13. Claims 5 & 6 either have typographical error or depend from cancelled claim 4.
14. Claim13 is objected to as word "range" is repeated twice in the end.
15. Claim 25 is objected to as the status of the claim indicates, "previously presented" however the claim is clearly amended.
16. Claim 34 is objected to as the status of the claim indicates, "Currently Amended" however the claim is clearly not amended.

Claim Rejections - 35 USC § 112, first paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. Claim 1-3, 5-11, 13-22, 24-42 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Claims disclose generating computer model based on a target model where the target model is created using the performance parameters – the disclosure lacks enablement for creating such a computer model effectively based on performance parameters, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. **Claim** 1-3, 5-11, 13-22, 24-42 **are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Regarding Claim 1-3, 5-11, 13-22, 24-42

Independent claims 1, 9, 14, 19, 24, 36 and 40 disclose limitation "first bound range" and "second bound range" for a "performance parameter". However no specific ranges are provided for this claim thereby failing to provide for the metes and bound for the ranges.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 1-27 & 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277hereafter) in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of applicant's own admission.

Regarding Claim 1 (Updated)

HE'277 *teaches a simulator* (HE'277: Col.4 Lines 61-Col.5 Line 6) *comprising: a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component* (HE'277: Col.6 Lines 58-62 – a transistor) *and has at least one performance attribute* (HE'277: Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15); *wherein the said computer model is generated based on the target model for said device* (HE'277: Col.6 Lines 58-62) *and wherein said target model is create using performance parameter ranges for the said performance attribute* (HE'277: Col.5 Lines 40-46; Also see ranges in KR'527 Fig.1 Elements 103-107). The transistor models are posynomial models, which are created (optimized) for one or more performance specifications (HE'277: Col.6 Lines 3-6). HE'277 further teaches, said target model *is adapted to determine the said target performance parameter range of said device* (HE'277: Col.5 Lines 27-35; Col.6 Lines 1-48; Also See KR'527 – Fig.1 element 109). HE'277 teaches *a processor in communication with the said memory and adapted to execute said computer model* (HE'277: Col.4 Lines 61-Col.5 Line 6; Col.6 Lines 58-67).

HE'277 teaches *target performance parameter range comprises multiple first bounded range* (due to process variation being modeled as inequalities - HE'277 –

single variation as function f_o and multiple variations as f_i - Col.7 Line 1-59; Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41) *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches *each of said first bounded ranges comprises performance parameters variations due to manufacturing process variations and is based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point* (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-60; Also See Col.20 Lines 27-60; performance point Col.21 Lines 35-49) and; HE'277 teaches said second bounded range *comprises performance parameters variations between designs for said design device* (HE'277: Col.11 Lines 40-Col.12 Line16) as variations in at least the Length and Width of the transistor.

HE'277 teaches *each of the multiple different designs is directed to a variation of a single design for the said integrated circuit*, as variation is topology to optimize various parameters (HE'277: Col.6 Lines 1-24). The second bound range is contrainted by these curves.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process where the performance parameter are current voltage switch point (See claim interpretation), although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example, **as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 2 (Updated)

HE'277 teaches that *multiple* designs are directed to variations of a single *design* (HE'277: Col.11 Lines 40-Col.12 Line16). For example changing the width (W) and lengths (L) of the transistors. These Length and Widths are constrained by most (Lmin, Wmin) and least linear (Lmax,Wmax) model curves.

Also See KR'527 Fig.1, wherein the element 110 has 4 points, two of them corresponding to process parameter variations making a bounded range and the other two related to lengths (design parameter).

Regarding Claim 3

HE'277 does not explicitly teach performance parameter *range* is the same for a target model of said device and a final hardware design of said device as the (performance) parameters are used for manufacturing and modeling. HE'277 also does not teaches interaction between the actual manufacturing and model simulation.

KR'527 teaches that performance parameter *range* is the same for a target model of said device and a final hardware design of said device (KR'527: Fig.6a, Fig.3) as the (performance) parameters are used for manufacturing and modeling.

KR'527 teaches in interaction between the actual manufacturing and model simulation (KR'527: Col.9-11).

Regarding Claim 5-7 (Updated)

HE'277 teaches using multiple constraints where the constraints vary as defined in the simulation, further HE'277 teaches performing tradeoff optimization between various constraints graphically displayed as curves (HE'277: Col.6 Lines 3-24). KR'527 also teaches statistical Monte Carlo based inputs (as ranges) & range correction (KR'527: Fig.6b, Col.12 Lines 8-50). Plurality of performance points (*range*) are selected as various input parameter values from statistical distributions mentioned above. Multiple first bound ranges can be seen in (KR'527: Fig.1) as well.

Regarding Claim 8 (Updated)

HE'277 teaches using geometric programming with its advantageous ability to solve thousands of constraints (HE'277: Col.5 Lines 6-35). Further, HE'277 teaches these constraints can be displayed as tradeoff (implying at least two constraints with plurality of evaluated results) in form of curve representing *target* performance parameters *range* with two-dimensional range of plurality of performance points (HE'277: Col.6 Lines 3-24; Also see KR'527: Col.12 Line 63-Col.13 Line 23).

Regarding Claim 9 (Updated)

Method claim 9 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 10 (Updated)

Method claim 10 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 11 (Updated)

Method claim 11 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 13 (Updated)

Method claim 13 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 14 & 15 (Updated)

Method claims 14 & 15 disclose similar limitations as claim 1 and are rejected for the same reasons as claim 1.

Limitation disclosed as "design goals" is further disclosed as "performance parameter". HE'277 teaches producing a target model (HE'277: Col.4 Lines 61-67). Further, KR'527 teaches developing a device and product based on the target model (KR'527: Fig.6a, Col.9-11 Section III). The goals for device and product are interpreted as same goal, as indicated in the preamble "a product comprising a device" shows that product only has one device. Although "comprising" does not limited the scope, design goals can be seen in HE'277 (Col.6 Lines 1-24).

KR'527 teaches target performance comprises plurality of performance points as points in the V/I curves (KR'527: Fig. 6c, Also see Fig.1 element 110). Further by

applicant's disclosure, the tools to predict process and design variations are known in the art (Specification: [0033]).

Regarding Claim 16 (Updated)

Method claim 16 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 17 (Updated)

Method claim 17 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 18 (Updated)

Method claim 18 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 19 (Updated)

Method claim 19 discloses similar limitations as updated claim 1 and is rejected for the same reasons as claim 1.

KR'527 teaches developing a design for the device based on the target model (in simulator) (KR'527: Fig. 6a). KR'527 further teaches modifications to design wherein modification comprises modifying a particular feature and adding a particular feature of the design (KR'527: Col.6 Lines 34-59). KR'527 teaches determining primary parameters for a particular feature; determining secondary parameters from the said primary parameters (KR'527: at least in Col.2 Lines 51-63; also in Fig.6a-b-c-element 680-615-618; Col.13 Lines 10-23 – I/V curve from L, T, N parameters).

KR'527: Col.2 Lines 51-63 states:

> Before an accurate model of semiconductor device 200 may be obtained, certain "parameters" must be extracted from semiconductor device 200, as illustrated in FIG. 1. Typically, a device simulator requires specific device "parameters" in order to provide a simulation. For example, one semiconductor device simulator requires five specific sets of parameters, as illustrated by parameters 103-107. Some of the parameters are extracted from device parameter extractor 102. Some of these parameters may correspond to physical measurements of transistor device 200, such as channel length L and doping concentration N+ ***[Primary parameters]***, while other parameters may be based on or derived from these physical measurements or other parameters ***[secondary parameters]***.

KR'527 teaches determining secondary parameters from said primary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 – I/V curve from L, T, N parameters) where the primary parameters are inputted into process simulator and secondary parameters are derived from primary parameters (element 680-615-618) and inputted into device simulator (Element 640).

KR'527 teaches balancing choices (KR'527: Col.2 Lines 20-24, Col.4 Lines 30-34) related to modification and particularly to primary and secondary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 – I/V curve from L, T, N parameters; element 680-615-618) so that target performance parameters will remain within first bound range and second bound range (KR'527: Abstract: Lines 19-27; Col.8 Lines 50-63).

Regarding Claim 20

KR'527 teaches correlating secondary parameters to at least one further secondary parameter (Col.2 Lines 51-63; Col.12 Lines 8-62; Fig.6a-c & 7 a-c).

Regarding Claim 21

KR'527 teaches verifying that all primary and secondary parameters are within allowable limits (Col.13 Lines 24-62).

Regarding Claim 22

HE'277 teaches specifying parameters as first order and second order (HE'277: Col.11 Line 59-Col.12 Line 15).

Regarding Claim 24

HE'277 teaches a method of developing a product (HE'277: Col.4 Lines 61-Col.5 Line 6) *comprising* a device with at least one performance attribute (HE'277: Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15) *wherein the said device comprises a integrated circuit component* (HE'277: Col.6 Lines 58-62 – as transistor) *and wherein said target model is create using performance parameter for the said performance attribute* (HE'277: Col.5 Lines 40-46). *The goals for device are based on the product* – i.e. size of the transistors is dependent on the goal of the amplified in HE'277 (HE'277: Col.6 Lines 1-24). HE'277 teaches *target performance parameter range includes a multiple first bounded range* (due to process variation being modeled as inequalities - HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34; Also see ranges in KR'527 Fig.1 Elements 103-107) *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches *target performance parameter range comprises multiple first bounded range*

(due to process variation being modeled as inequalities - HE'277 – single variation as function f_o and multiple variations as f_j - Col.7 Line 1-59; Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41) *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches *each of said first bounded ranges comprises performance parameters variations due to manufacturing process variations and is based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point* (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-60; Also See Col.20 Lines 27-60; performance point Col.21 Lines 35-49) and; HE'277 teaches said second bounded range *comprises performance parameters variations between designs for said design device* (HE'277: Col.11 Lines 40-Col.12 Line16) as variations in at least the Length and Width of the transistor.

HE'277 teaches *each of the multiple different designs is directed to a variation of a single design for the said integrated circuit*, as variation is topology to optimize various parameters (HE'277: Col.6 Lines 1-24). The second bound range is contrainted by these curves.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process *where the performance parameter are current voltage switch point*, although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided as V/I Curves (Abstract: Lines 19-27; Col.8 Lines 50-63). The simulator simulates the computer model, created in the simulator, of the said product to determine if the product/device goals are met (KR'527: Fig.6a-6c).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277

discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example**, as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 25 (Updated)

Method claim 25 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 26

Method claim 26 discloses similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 27

KR'527 teaches the step of accepting altered device design further comprises the steps of carrying out experiments on test chips (KR'527: Fig.3, actual to simulated data comparison & guard band generation Col.13 Lines 32-62).

Regarding Claim 30

KR'527 teaches calculating a primary parameter from a physical device feature as L, T and N values (KR'527: Col.11 at least in Lines 19-27); correlating a secondary parameter from said primary parameter as associating resulting I/V curve with the L, T, N values (KR'527: Col.13 Lines 10-23); *calculating secondary parameter based on the primary parameters based on predetermined primary to secondary correlation*

I/V curve based on L, T, and N value equation (KR'527: Col.13 Lines 10-23; Fig. 6c; HE'277; Equation 16); and comparing said secondary parameter to said target performance parameter (KR'527: Col.13 Lines 24-37).

Regarding Claim 31

KR'527 teaches correlating other secondary parameters from correlations to said secondary parameters as correlating the V/I curve to the various channel length and attributes (short, short long etc) (KR'527: Fig 5a, Element 500).

Regarding Claim 32

KR'527 teaches primary parameter is directly related to physical device feature as related to channel length, doping, gate oxide thickness (KR'527: Col.11 at least in Lines 19-27 & Table C).

Regarding Claim 33

KR'527 teaches correlating primary to secondary parameters (KR'527: Fig 5a, Element 500). Secondary parameters could be derived parameters like "beta" whose derivation using equation is well known in the art.

Regarding Claim 34

Method claim 34 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 35 (Updated)

Method claim 35 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 36 (Updated)

Product claim 36 discloses similar limitations as updated claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product as alternate embodiment (HE'277: Col.22 Lines 1-21).

Regarding Claim 37 (Updated)

Product claim 37 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 38

Method claim 38 discloses similar limitations as claim 7 and is rejected for the same reasons as claim 7.

Regarding Claim 39

Method claim 39 discloses similar limitations as claim 8 and is rejected for the same reasons as claim 8.

Regarding Claim 40

Method claim 40 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product (storage device) readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method (HE'277: Col.22 Lines 1-21).

Regarding Claim 41 (New)

HE'277 teaches that *multiple* designs are directed to variations of a single *design* (HE'277: Col.11 Lines 40-Col.12 Line16). For example changing the width (W) and lengths (L) of the transistors. These Length and Widths are constrained by most (Lmin, Wmin) and least linear (Lmax,Wmax) model curves.

Also See KR'527 Fig.1, wherein the element 110 has 4 points, two of them corresponding to process parameter variations making a bounded range and the other two related to lengths (design parameter).

Regarding Claim 42 (New)

HE'277 teaches computer-implemented method (HE'277: Col.4 Lines 61-Col.5 Line 6) of developing a product comprising a device with at least one performance attribute (HE'277: Col.6 Lines 1-24), wherein said device comprises an integrated circuit component (HE'277: Col.6 Lines 58-62 – a transistor), said method comprising: designing said product using a computer model that is based on a target model of said device, wherein said target model is created using said a target performance parameter range for said performance attribute (HE'277: Col.6 Lines 1-24), wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range (HE'277: Col.5 Lines 27-35, 40-46; Also see ranges in KR'527 Fig.1 Elements 103-107), wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance

point, wherein each of said multiple different designs is directed to a variation of a single design for said device (due to process variation being modeled as inequalities - HE'277 – single variation as function f_0 and multiple variations as f_j - Col.7 Line 1-59; Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41, HE'277: Col.6 Lines 1-24), wherein said second bounded range is constrained is constrained (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48) by a most linear of said multiple model curves mad a least linear of said multiple model curves (Also See KR'527: Fig.1 Element 110) and Wherein target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bound range around said least linear of said multiple model curves (Also See KR'527: Fig.1 Element 110).

Motivation to combine HE'277 with KR'527 is same as in claim 1.

19. Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277 hereafter), in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of applicant's own admission, further in view of U.S. Patent No. 6,028,994 issued to Peng et al (PE'994 hereafter).

Regarding Claim 28 & 29

Teaching of HE'277, KR'527 and applicant's own admission are shown in claim 24 rejections above.

HE'277 & KR'527 do not teach design goals for product, developing product fro from target model and product model simulation & alteration based on feedback.

PE'994 teaches teach design goals for product (PE'994: Col.2 Line 49-59 – predicted performance), developing product from target model as combined product & device model represented by product performance model (PPM) (PE'994: Fig. 1; Col.6 Lines 57-67) and product model simulation & alteration based on feedback as self learning (PE'994: Fig.1 Step 64). The product is represented as package of wafer chip and the device is represented as wafer chip (PE'994: See Fig.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of PE'994 to HE'277 & KR'527. The motivation to combine would have been that HE'277 & KR'527 and PE'994 are attempting to design a model that can mimic and or predict the performance of the semiconductor model (PE'994: Abstract; HE'277 & KR'527: Abstracts) based on the input parameters. Further, teaches PE'994 specifying the

input parameters as ranges (PE'994: Fig.3 Col.5 Lines 35-48) for performance which is very similar to the KR'527 teachings disclosed before relating to ranges for performance parameters.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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